Translation

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-027827

(43)Date of publication of application : 27.01.1998

(51)Int.Cl. H01L 21/60
H01L 23/12
// H01L 21/301

(21)Application number : 08-180400

(22)Date of filing : 10.07.1996

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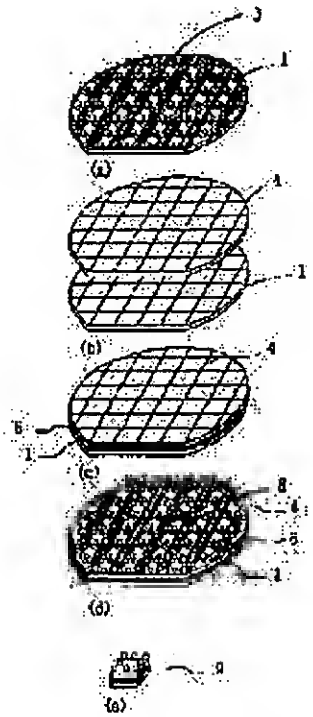
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method of manufacturing a semiconductor device, which makes equal substantially the size of a semiconductor chip with the size of a base substrate to contrive a miniaturization of the device and moreover, facilitates a mounting and makes a mass productivity superior.

SOLUTION: Electrode parts on a ceramic base substrate 4 of the same shape substantially with the shape of a silicon wafer 1 are conformed to plated bumps 3 formed on the wafer 1 to connect electrically the wafer 1 with the base substrate 4. Then, an epoxy resin 6 is injected in the gap between the wafer 1 and the substrate 4 and is cured to seal the gap. After metal bumps 8 are formed on the substrate 4 in an area shape, the wafer 1 and the substrate 4 are batch-diced on the same cutting surface. Moreover, when the wafer 1 and the substrate 4 are sealed, an anisotropic conductive film may be used.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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DETAILED DESCRIPTION

[Detailed description]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the manufacture technique of a semiconductor device of having a chip size package among semiconductor devices.
[0002]
[Prior art] In recent years, it is asked for a miniaturization and high-density-izing of a semiconductor device in connection with the spread of pocket information devices, such as PHS (Personal Handyphone System) and PDA (Personal Digital Asistant). The chip size package (CSP) with almost equal size of a semiconductor chip and size of a package is raised as a means of this high-density-izing.
[0003] The semiconductor device which has the conventional chip size package is explained with reference to drawing 5 and drawing 6 . The cross section of the semiconductor device by the flip chip bonding of the former [drawing 5] and drawing 6 are the cross sections of the semiconductor device by the conventional TAB formula.
[0004] First, the conventional semiconductor device by flip chip bonding is explained. First, as shown in drawing 5 , the metal bump 102 is formed in the polar zone of the rear face of the semiconductor chip 101 which carried out the dicing of the semiconductor wafer and piece[of an individual]-ized it. Next, the polar zone of a semiconductor chip 101 and the polar zone of the top of the base substrate 103 of a ceramic are electrically connected through this metal bump 102. Next, by the resin 104, potting of the clearance of a semiconductor chip 101 and the base substrate 103 is carried out, and it is ****ed. Then, the metal bump 105 is formed in the polar zone of the rear face of the base substrate 103.
[0005] Next, the conventional semiconductor device by TAB formula is explained. First, as shown in drawing 6 , inner-lead-bonding connection with the TAB tape 112 which has lead 113 to the semiconductor chip 111 which carried out the dicing of the semiconductor wafer and piece[of an individual]-ized it, and the periphery is made. Next, the periphery is enclosed by the dam frame 114 which is the protect ring of a semiconductor chip 111, and the interior is ****ed by the resin 115. Then, the metal bump 116 is formed in the rear face of the TAB tape 112.
[0006]
[Object of the Invention] although potting of the clearance of a semiconductor chip 101 and the base substrate 103 is carried out and it is ****ed by the resin 104, in order that the chip size package by flip chip bonding may take care of the metal bump 102 conventionally -- the liquid at the time of potting -- in order to prevent whom, the base substrate 103 big about 2mm is needed from 1mm to a semiconductor chip 101, and there was a problem that the size of the base substrate 103 will become large to a semiconductor chip 101
[0007] Moreover, since the bump area for a package became small and the bump pitch became narrow in order to use the TAB tape 112 with a size smaller than a semiconductor chip 111, the chip size package by TAB formula had the problem that a package became difficult.
[0008] Moreover, since it assembled to every one of a semiconductor chip 101,111 and a process was needed after both do the dicing of the semiconductor wafer and piece[of an individual]-ize a

semiconductor chip 101,111, the manufacture of a semiconductor device took time and there was a problem that it was necessary to prepare tools, such as a positioning, for every chip size, further.
[0009] In consideration of the above situations, the size of this invention of a semiconductor chip and a base substrate is substantially equal, and it is easy to mount and is aimed at offering the manufacture technique of a semiconductor device of having the chip size package excellent in mass-production nature.
[0010]
[The means for solving a technical problem] In order to attain the above-mentioned purpose the manufacture technique of the semiconductor device of this invention The process which prepares the base substrate of the same configuration substantially with a semiconductor wafer, and the process which forms a metal bump in the polar zone of the aforementioned semiconductor wafer, The process which connects electrically the polar zone of the aforementioned semiconductor wafer, and the polar zone of the top of the aforementioned base substrate through the aforementioned metal bump, It is characterized by providing the process which ****s the clearance of the aforementioned semiconductor wafer and the aforementioned base substrate by the resin, the process which forms a metal bump in the polar zone of the rear face of the aforementioned base substrate, and the process which carries out the dicing of the aforementioned semiconductor wafer, a resin, and the base substrate.
[0011] Furthermore, in the process which carries out the dicing of the aforementioned semiconductor wafer, a resin, and the base substrate, it is desirable to cut the aforementioned semiconductor wafer, a resin, and a base substrate by the same cut surface.
[0012] Furthermore, as for the aforementioned resin, it is good to be the potting resin of hypoviscosity. Moreover, the process which prepares the base substrate of the same configuration substantially with a semiconductor wafer, The process which forms a metal bump in the polar zone of the aforementioned semiconductor wafer, and the process which prepares the anisotropy electric conduction layer of the same configuration substantially with the aforementioned semiconductor wafer and a base substrate, In order to connect electrically the polar zone of the aforementioned semiconductor wafer, and the polar zone of the aforementioned base substrate The process which inserts the aforementioned anisotropy electric conduction layer between the aforementioned semiconductor wafer and the aforementioned base substrate, and fixes, There is the manufacture technique of the semiconductor device characterized by providing the process which forms a metal bump in the polar zone of the rear face of the aforementioned base substrate, and the process which carries out the dicing of the aforementioned semiconductor wafer, a resin, and the base substrate collectively. Furthermore, as for the aforementioned anisotropy electric conduction layer, it is desirable that it is an epoxy resin.
[0013]
[Gestalt of implementation of invention] Hereafter, the semiconductor device applied to the gestalt of enforcement of the 1st of this invention with reference to a drawing and its manufacture technique are explained. Drawing 1 is [the gestalt of enforcement of the 1st of this invention / the cross section of the manufacturing process of such a semiconductor device and drawing 3 of the manufacturing-process view of such a semiconductor device and drawing 2] the enlarged views of the cross section of such a semiconductor device in the gestalt of enforcement of the 1st of this invention at the gestalt of enforcement of the 1st of this invention.
[0014] First, as shown in drawing 1 (a) and drawing 2 (a), the plating bump 3 is formed in the polar zone 2 of the top of the silicon wafer 1 before carrying out dicing. Next, as shown in drawing 1 (b) and drawing 2 (b), the polar zone 5 of the rear face of the base substrate 4 of the ceramic of the same configuration is doubled with the plating bump 3 formed on the silicon wafer 1 as substantially as a silicon wafer 1. Next, a silicon wafer 1 and the base substrate 4 are electrically connected through the plating bump 3.
[0015] Next, as shown in drawing 1 (c) and drawing 2 (c), the epoxy resin 6 of hypoviscosity is poured into the clearance of a silicon wafer 1 and the base substrate 4 using a capillarity. Then, heat is applied and an epoxy resin 6 is stiffened. Consequently, as shown in drawing 3 , the clearance of a silicon wafer 1 and the base substrate 4 is ****ed by the epoxy resin 6.

[0016] Next, as shown in drawing 1 (d) and drawing 2 (d), the metal bump 8 of solder is formed in the polar zone 7 of the top of the base substrate 4 in the shape of an area. Next, as shown in drawing 1 (e) and drawing 2 (e), dicing is performed and it piece[of an individual]-izes to the semiconductor device which carried the semiconductor chip 9 respectively.
[0017] By the above, the manufacturing process of such a semiconductor device is completed in the gestalt of enforcement of the 1st of this invention. In order to carry out the dicing of a silicon wafer 1 and the base substrate 4 collectively by the same cut surface, it is possible for the size of a semiconductor chip 9 and the base substrate 4 to become equal, and to realize a miniaturization of a semiconductor device.
[0018] Moreover, until it forms the metal bump 8 for a package is put in block on the top of the base substrate 4 per wafer, and is processed into it, and since the tool depending on the chip size is unnecessary, it excels in mass-production nature.
[0019] Moreover, if it has the viscosity which can use a capillarity, it is possible for it not to be limited to the gestalt of implementation of the above 1st, but to **** the clearance of a silicon wafer 1 and the base substrate 4 even if it uses which resin.
[0020] Next, the manufacture technique of such a semiconductor device is explained to the gestalt of enforcement of the 2nd of this invention with reference to drawing 4 . Drawing 4 (a) is explanatory drawing of such a semiconductor device, and drawing 4 (b) is [the gestalt of enforcement of the 2nd of this invention] the enlarged view of the cross section of such a semiconductor device at the gestalt of enforcement of the 2nd of this invention.
[0021] Since it is the same as that of the process shown in drawing 1 (a) and drawing 2 (a) of the gestalt of the 1st enforcement until it forms the plating bump 3 in the top of a silicon wafer 1, it omits. After forming the plating bump 3, the anisotropy electric conduction layer 10 of the epoxy resin 12 which was substantially used as the silicon wafer 1 and the base substrate 4 at the same configuration and which contained the metals 11, such as nickel with a diameter of about 5 micrometers, for example is prepared. This anisotropy electric conduction layer 10 is inserted between a silicon wafer 1 and the base substrate 4, and heat is applied and stiffened. Consequently, a silicon wafer 1 and the base substrate 4 fix.
[0022] Then, since it is the same as that of the process of drawing 1 (d) in the gestalt of the 1st enforcement, and drawing 1 (e) until it carries out dicing, it omits. If a pressure is applied, the resin 12 of the fraction will be compressed, and the anisotropy electric conduction layer 10 has the property in which the metal 11 contained in the resin 12 gathers. Therefore, since a pressure is applied to the anisotropy electric conduction layer 10 of the fraction which touches the plating bump 3 formed in the silicon wafer 1 when it inserts between a silicon wafer 1 and the base substrate 4, as shown in drawing 4 (b), the metal 11 of the fraction gathers in the plating bump's 3 upper part. Then, if heat is applied, the plating bump 3 and the metal 11 will connect, and further, since the polar zone 5 of the top of the base substrate 4 connects with a metal 11, a silicon wafer 1 and the base substrate 4 will be electrically connected as a result.
[0023] Since the resin seal of the clearance of a silicon wafer 1 and the base substrate 4 can be performed while performing electrical installation of a silicon wafer 1 and the base substrate 4 by using this anisotropy electric conduction layer 10, it is possible to cut down the number of manufacturing processes.
[0024] Moreover, it is not limited to the gestalt of implementation of the above 2nd, but if the resin 12 of the anisotropy electric conduction layer 10 is a thermosetting thing, every thing is possible for it. Moreover, the modality and size of a metal 11 which are contained in the anisotropy electric conduction layer 10 are not limited to the gestalt of implementation of the above 2nd. In addition, this invention is not limited to the gestalt of the above 1st and the 2nd implementation, but may use things other than a ceramic for the base substrate 4.
[0025]
[Effect of the invention] Since according to this invention a miniaturization of a chip size package is realized, and it bundles up per wafer, it assembles and a process is performed in order to carry out the dicing of a semiconductor wafer and the base substrate by the same cut surface, the manufacture

technique of a semiconductor device excellent in mass-production nature can be offered.

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CLAIMS

[Claim]
[Claim 1] The process which prepares the base substrate of the same configuration substantially with a semiconductor wafer, and the process which forms a metal bump in the polar zone of the aforementioned semiconductor wafer, The process which connects electrically the polar zone of the aforementioned semiconductor wafer, and the polar zone of the top of the aforementioned base substrate through the aforementioned metal bump, The manufacture technique of the semiconductor device characterized by providing the process which ****s the clearance of the aforementioned semiconductor wafer and the aforementioned base substrate by the resin, the process which forms a metal bump in the polar zone of the rear face of the aforementioned base substrate, and the process which carries out the dicing of the aforementioned semiconductor wafer, a resin, and the base substrate.
[Claim 2] The manufacture technique of the semiconductor device the claim 1 publication characterized by cutting the aforementioned semiconductor wafer, a resin, and a base substrate by the same cut surface in the process which carries out the dicing of the aforementioned semiconductor wafer, a resin, and the base substrate.
[Claim 3] The aforementioned resin is the manufacture technique of the semiconductor device the claim 1 publication characterized by being a potting resin.
[Claim 4] The process which prepares the base substrate of the same configuration substantially with a semiconductor wafer, and the process which forms a metal bump in the polar zone of the aforementioned semiconductor wafer, In order to connect electrically the process which prepares the anisotropy electric conduction layer of the same configuration substantially with the aforementioned semiconductor wafer and a base substrate, and the polar zone of the aforementioned semiconductor wafer and the polar zone of the aforementioned base substrate The process which inserts the aforementioned anisotropy electric conduction layer between the aforementioned semiconductor wafer and the aforementioned base substrate, and fixes, The manufacture technique of the semiconductor device characterized by providing the process which forms a metal bump in the polar zone of the rear face of the aforementioned base substrate, and the process which carries out the dicing of the aforementioned semiconductor wafer, a resin, and the base substrate collectively.
[Claim 5] The aforementioned anisotropy electric conduction layer is the manufacture technique of the semiconductor device the claim 4 publication characterized by being an epoxy resin.

[Translation done.]